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(54) Electronic switching circuit for reducing power-on switching transients

Elektronischer Schaltkreis zur Transientenminderung beim Einschalten

Circuit électronique de réduction de transients dans le déclenchment

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Description

[0001] The present invention relates to an electronic switching circuit for reducing power-on switching transients.

[0002] Number 1 in Figure 1 indicates a known electronic switching circuit in which a first solid-state electronic switch 3, e.g. defined by an IGBT transistor, has a first terminal 3a connected to a voltage source Val via an inductor L1; a second terminal 3b connected via an inductor L2 to a first terminal of a load 5 shown schematically by an inductor Lc and a resistor Zc connected in series with each other; and a control terminal 3c conveniently defined by the gate terminal of the IGBT transistor, and which is supplied via a control resistor Rg with a control signal C. The binary control signal C (Figure 2a) may be defined by a voltage varying between a first logic state (e.g. a zero or negative voltage) corresponding to opening of electronic switch 3, and a second logic state (e.g. a positive voltage Vc) corresponding to closing of electronic switch 3; and electronic switch 3 is connected in parallel to a recirculating diode Dc1 having the cathode connected to terminal 3a and the anode connected to terminal 3b.

[0003] The electronic switching circuit also comprises a second solid-state electronic switch 7 also defined by an IGBT transistor, and which has a first terminal 7a connected to the first terminal of load 5; a second terminal 7b connected to a reference voltage Vref to which a second terminal of load 5 is also connected; and a control terminal 7c supplied via a control resistor Rg with a control signal preferably but not exclusively opposite to control signal C. Electronic switch 7 is also connected in parallel to a recirculating diode Dc2 having the cathode connected to terminal 7a and the anode connected to terminal 7b.

[0004] The above circuit may conveniently define a CHOPPER for dividing the direct supply voltage Val and supplying load 5 (e.g. comprising an electric motor) with a pulsating voltage; and the CHOPPER circuit may be combined with another of the same type to supply a load with alternating current and so define an INVERTER.

[0005] Known electronic switching circuits present a drawback when turned on, due to the physical behaviour of diode Dc2. That is, when switch 3 is open and switch 7 closed (low logic value of control signal C), the loop defined by load 5 and recirculating diode Dc2 is supplied with recirculating current by inductor Lc forming part of the loop; and, when switch 3 is closed, diode Dc2 is reverse biased and should therefore be turned off. In actual fact, however, when switch 3 is turned on, the current Ic supplied by diode Dc2 decreases substantially steadily to begin with (first portion T1 in Figure 2b), and, on reaching the zero value Ico (at which it should stop decreasing if diode Dc2 were to perform ideally), continues to fall (portion T2) to a negative value Ir from which it then returns to the zero value Ico, thus creating in diode Dc2 a negative current peak Ir induced by reverse conduction (recovery) of the diode. As a result, the current Ig supplied by switch 3 and equal to the sum of the load current and current Ic of the diode (Figure 2c) increases substantially steadily at portion T1, and, on reaching the steady-state value (at which it should stop increasing if diode Dc2 were to perform ideally), continues rising (portion T2) up to a positive value Ip from which it then falls back to the steady-state value, thus creating in switch 3 a positive current peak Ip induced by reverse conduction of diode Dc2.

[0006] Diode recovery is a well known phenomenon which has always been considered uncontrollable, and which, on account of the current peak Ir applied to diode Dc2 and the normally high supply voltages of such electronic circuits, results in the generation of extremely high instantaneous power capable of destroying the diode. For example, supply voltages of thousands of volts (e.g. 2000 V) may result in recovery currents of about a thousand amperes (e.g. 1500 A) and an instantaneous power of several megawatts (e.g. 3 MW) which no diode on the market could withstand. Similarly, the high current supplied by switch 3 may either damage the switch itself or at least cause it to operate, albeit for a few instants, outside the safety range.

[0007] The known solution to the above drawbacks is to prolong the turn-on time of electronic switch 3 to gradually reduce the current in diode Dc2 and so achieve lower recovery current values by selecting a sufficiently high resistance of resistor Rg. Electronic switch manufacturers, in fact, specify a minimum resistance of resistor Rg for safeguarding against the recovery phenomenon. Prolonging the turn-on time of electronic switches, however, clearly results in a drastic increase in the amount of energy dissipated each time the circuit switches.

[0008] It is an object of the present invention to provide a switching circuit of the above type, designed to solve the recovery phenomenon with a minimum increase in the amount of energy dissipated by switching of the circuit.

[0009] According to the present invention, there is provided an electronic switching circuit for reducing power-on switching transients, and as described in Claim 1.

[0010] The present invention also relates to a method of controlling an electronic switching circuit, and as described in Claim 11.

[0011] A non-limiting embodiment of the present invention will be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a known solid-state electronic switching circuit;

Figures 2a, 2b, 2c show waveforms of quantities relative to the Figure 1 circuit;

Figure 3 shows a solid-state electronic switching circuit for reducing power-on switching transients in accordance with the teachings of the present inven-

tion;

Figures 4a, 4b, 4c show waveforms of quantities relative to the Figure 3 circuit;

Figure 5 shows a detailed portion of the Figure 3 circuit;

Figures 6a-6f show waveforms of quantities relative to the Figure 5 circuit.

[0012] With reference to Figure 3, number 10 indicates an electronic switching circuit wherein a first solid-state electronic switch 13, e.g. defined by an IGBT transistor, has a first terminal (collector terminal) 13a connected to a direct voltage source Val; a second terminal (emitter terminal) 13b communicating with a first terminal 15a of a load 15 (e.g. a direct-current electric motor) shown schematically by an inductor Lc and a resistor Zc connected in series to each other; and a control terminal 13c conveniently defined by the gate terminal of the IGBT transistor, and which is supplied via an active control circuit 17 with a control signal C. More specifically, active control circuit 17 comprises an input 17a supplied directly with control signal C; and an output 17b connected to control terminal 13c.

[0013] The binary control signal C (Figure 4a) is conveniently defined by a voltage varying between a first value C_1 (e.g. -15 V) corresponding to opening of electronic switch 13, and a second value C_2 (e.g. +15 V) for closing electronic switch 13; and electronic switch 13 is connected in parallel to a recirculating diode 20 having the cathode connected to terminal 13a and the anode connected to terminal 13b.

[0014] Electronic switching circuit 10 also comprises a second solid-state electronic switch 27 also defined by an IGBT transistor, and which has a first terminal 27a (collector terminal of the IGBT transistor) communicating with terminal 13b, and a second terminal 27b (emitter terminal of the IGBT transistor) connected to a reference voltage to which a second terminal 15b of load 15 is also connected.

[0015] Electronic switch 27 is also connected in parallel to a recirculating diode 30 having the cathode connected to terminal 27a and the anode connected to terminal 27b.

[0016] Second switch 27 also comprises a control terminal 27c (gate terminal of the IGBT transistor) supplied with a second control signal Cz, which may be correlated to control signal C. In the above CHOPPER configuration, signal Cs is always in the block state, i.e. switch 27 is always open and only recirculating diode 30 is operative.

[0017] According to the present invention, circuit 10 comprises a current transducer 33 interposed between terminal 13b and a node 34 to which terminal 27a of second switch 27 and first terminal 15a of load 15 are connected.

[0018] The current Ig flowing in switch 13 during closure of the switch, and which, as stated, equals the current flow in load 15 plus the recovery current Ic of diode 30 (Figure 2c), flows through current transducer 33, which generates a control signal Vcnt proportional to the derivative of current Ig, i.e.:

$$Vcnt = \frac{d(Ig)}{dt}$$

[0019] Control signal Vcnt is conveniently supplied to control circuit 17 in which it is compared by a comparator 36 with a threshold value Vth to generate a binary output signal T (Figure 4b) assuming a first and a second logic state T1, T2 when control signal Vcnt is respectively above and below threshold value Vth. Control circuit 17 also comprises a power-on control device 38 (shown schematically by a switch) interposed between input 17a and output 17b and controlled by binary signal T. When binary signal T assumes second logic state T2, i.e. when the derivative of current Ig is below threshold Vth, power-on control device 38 (switch 38 closed) allows control signal C controlling closure of switch 13 to be transferred through device 17 to the gate of the IGBT transistor. Conversely, when binary signal T assumes first logic state T1, i.e. when the derivative of current Ig is above threshold Vth, power-on control device 38 (switch 38 open) prevents control signal C controlling closure of switch 13 from being applied to the gate of the IGBT transistor, and so prevents switch 13 from being turned on.

[0020] In actual use, under normal operating conditions, i.e. when the derivative of current Ig is below threshold value Vth, control signal C applied to input 17a is transferred to output 17b and contributes in known manner towards controlling electronic switch 13 (portion C' of the control signal shown in Figure 4c). More specifically, IGBT transistor 13 is kept open for values C_1 and is closed for values C_2 of control signal C. When IGBT transistor 13 is closed, the recirculating current Ic flowing in diode 30 decreases rapidly and, due to the recovery phenomenon mentioned above, tends towards negative value Ir; and the rapid variation in recirculating current Ic produces a rapid increase in current Ig across switch 13. The increase in current Ig, however, is detected by transducer 33, which, as stated, generates a control signal Vcnt indicating the variation in time of the current across switch 13. When the derivative of current Ig is above threshold value Vth, i.e. when current Ic falls too rapidly on account of the recovery phenomenon, the control signal is prevented (switch 38 open) from being transferred to transistor 13, and the previous control signal controlling closure of transistor 13 is removed, so that IGBT transistor 13 passes from a "hard" power-on state, i.e. with a high current derivative (switch 13 closing rapidly), to a "soft" power-on state, i.e. with a much lower current derivative, to prevent any further reduction in the recirculating current. IGBT transistors, in fact, are known to comprise, between the gate and emitter terminals, a parasitic capacitance Cp high enough, when charged, to maintain the GATE potential at a sufficiently

high positive value Vt even when no control signal is applied to the GATE. As such, when control signal C to the gate of transistor 13 is removed, the gate nevertheless remains biased at voltage Vt by the parasitic capacitance, but the IGBT transistor is no longer saturated and operates in the linear zone.

[0021] The recirculating current may therefore return to lower absolute values, and, when the derivative of current Ig also falls below the threshold value, closure of switch 13 is once again enabled (control signal C") and the switch may once more be closed is so controlled by control signal C.

[0022] Figure 5 shows an actual physical embodiment of the circuit shown schematically in Figure 3.

[0023] In the example shown, current transducer 33 for generating an output signal proportional to the derivative of current Ig across transducer 33 is defined by a straightforward inductor interposed between terminal 13b and node 34, and the voltage Vcnt at the terminals of which is known to be given by the following equation:

$$Vcnt = L\frac{d(Ig)}{dt}$$

where Ig is the current across the inductor, and L the inductance of inductor 33.

[0024] Inductor 33 is conveniently defined by the parasitic inductance in the physical IGBT component between the control return terminal (auxiliary emitter - 13b) and the power terminal (power emitter - node 34). The physical IGBT transistor, in fact, is known to comprise a casing with four connection terminals respectively corresponding to the collector terminal (13a), the control (GATE) terminal (13c), the control return terminal (auxiliary emitter - 13b) connected directly to the emitter region of the CHIP defining the IGBT transistor, and the power terminal (power emitter - node 34) through which the IGBT transistor current flows.

[0025] Comparator 36 in turn comprises a PNP transistor 40 with the emitter connected to auxiliary emitter 13b, and the collector connected via a resistor 42 to a negative reference voltage Vref (e.g. -15 V); a resistor 43 interposed between the emitter and base of transistor 40; and a resistor 44 having a first terminal connected to the base of transistor 40, and a second terminal to which is applied a reference voltage Vth conveniently defined by the voltage drop at the terminals of a Zener diode 46 and a diode 47 connected in series with each other and interposed between the base of transistor 40 and node 34. Conveniently, the cathode of Zener diode 46 is connected to resistor 44, and the cathode of diode 47 is connected to node 34. The output of comparator 36 is defined by the collector of transistor 40, to which is connected the input of an inverting circuit 50 forming part of power-on control device 38, which also comprises an AND gate 52 having a first input 52a communicating with the output of inverting circuit 50, a second input 52b supplied with control signal C, and an output 52c communicating, via a level shift circuit 54, with control terminal 13c of electronic switch 13.

[0026] Level shift circuit 54 comprises an inverting level shifter 61 having an input connected to output 52c of AND gate 52, and an output connected to the gate of a first P-channel MOSFET transistor 57, which has the source terminal connected to a positive direct voltage source (+15 V), and the drain terminal connected to a first terminal of a resistor 58, the second terminal of which is connected to a first terminal of a resistor 59. Resistor 59 has a second terminal connected to the source terminal of an N-channel MOSFET transistor 60, the drain terminal of which is connected to a negative direct voltage source (-15 V). Inverting level shifter 61 provides for converting a -15 V input voltage (logic 0) into a +15 V output voltage, and for converting a zero volt input voltage (logic 1) into a zero volt output voltage. Active control circuit 17 also comprises an inverting circuit 62 having an input receiving control signal C, and an output connected to the GATE terminal of transistor 60. Node 63 connecting resistors 58 and 59 defines the output of level shift circuit 54, which is connected to control terminal 13c over an electric line 64.

[0027] In actual use, under normal operating conditions, i.e. when voltage Vcnt of inductor 33 is lower than voltage Vth, transistor 40 is reverse biased and does not conduct, so that the voltage V1 at the collector of transistor 40 equals -15 V, equivalent to a logic 0 (Figure 6b). The logic 0 (-15 V) applied to the input of inverting circuit 50 is then converted into a signal V2 (Figure 6c) representing a logic 1 (of a conventional value, say, of 0 V) applied to input 52a of AND gate 52, which generates an output signal A (Figure 6d) representing a logic state equal to the product of the logic 1 state multiplied by the logic state applied to input 52b. More specifically, if signal C (Figure 6a) assumes a logic value C_2 equal to a logic 1 (conveniently equal to 0 V), output A of gate 52 also assumes a logic 1 value; and, if signal C assumes a logic value C_1 equal to a logic 0 (conveniently equal to -15 V), the output of gate 52 also assumes a logic 0 value. The logic 1 at the output of gate 52 is converted by shift circuit 54 into a +15 V signal G (Figure 6f) for closing IGBT transistor 13, and the logic 0 at the output of gate 52 is converted by shift circuit 54 into an open-circuit condition of IGBT transistor 13.

[0028] In fact, with a logic 1 (0 V) at the input of inverting level shifter 61, the output of inverting level shifter 61 equals 0 V, transistor 57 is conductive, and node 63 is supplied with a voltage of +15 V, which, applied to gate 13c, saturates and turns on IGBT transistor 13. In which case, a logic 1 is supplied to the input of inverting circuit 62, which produces an output voltage of -15 V (equivalent to a logic 0) to disable transistor 60.

[0029] With a logic 0 (-15 V) at the input of inverting level shifter 61, the output of inverting level shifter 61 equals +15 V, which, applied to transistor 57, disables transistor 57 so that the logic 0 applied to the input of circuit 62 forces the output of circuit 62 to a voltage value

(0 in) equivalent to a logic 1 applied to the gate of transistor 60, which so conducts that the -15 V voltage is applied to gate 13c to disable and turn off IGBT transistor 13.

[0030] Under normal operating conditions, therefore, switch 13 is closed by a logic 1 and opened by a logic 0 of signal C.

[0031] The diode recovery phenomenon causes the voltage Vcnt of inductor 33 to exceed voltage Vth, so that transistor 40 is biased directly and made conductive, and the voltage at the collector of transistor 40 equals 0 V, equivalent to a logic 1. The logic 1 (0 V) applied to the input of inverting circuit 50 is then converted into a logic 0 (-15 V) applied to input 52a of AND gate 52, which generates an output signal of a logic state equal to the product of input 52b multiplied by the 0 logic state. More specifically, the output of AND gate 52 is always at logic 0 regardless of whether signal C assumes a logic 1 (0 V) or a logic 0 (-15 V), and the logic 0 present at all times at the output of gate 52 is converted by inverting level shifter 61 into a +15 V signal applied to MOSFET transistor 57, which opens, leaving gate terminal 58 floating, so that transistor 13 cannot be closed. In which case, if control signal C assumes a logic 1, the output of circuit 62 assumes a logic 0 (-15 V) and transistor 60 is nonconductive; if control signal C assumes a logic 0, the output of circuit 62 assumes a logic 1 (0 V), and transistor 60 conducts to supply gate 13c with a negative -15 V voltage, so that transistor 13 may nevertheless be opened.

[0032] In other words, a logic 0 at the output of circuit 50 prevents transistor 13 from being turned on by preventing transfer of control signal C from input 17a to control terminal 13c, but allows the transistor to be turned off.

[0033] The advantages of the present invention will be clear from the foregoing description. In particular, active control circuit 17 provides, fully automatically and by means of a highly straightforward circuit, for preventing application of the closing signal to switch 13 whenever the current in recirculating diode 30 moves rapidly towards "critical" values immediately interrupting the increase (towards negative values) of the diode current when switch 13 is set to the linear operating region.

[0034] Together with inverting circuit 50, comparator 36 in fact alternately generates a disabling signal (signal V2 = logic 0) when control signal Vcnt exceeds threshold Vth, and an enabling signal (signal V2 = logic 1) when control signal Vcnt is below threshold Vth.

[0035] Upon safe operating conditions being restored, i.e. when the recirculating current stops increasing, the conditions previous to the transient state caused by recovery of the diode are restored, and switch 13 may once more be closed by signal C. In the presence of the enabling signal (V2 = logic 1), power-on control device 38 in fact provides for enabling control of first switch 13 by control signal C.

[0036] Circuit 10 may also comprise (Figure 5) a biasing circuit 70 having an output 70a communicating with control terminal 13c, and an enabling input 70b communicating with the output of inverting circuit 50; which circuit 70 is activated by a logic 0 at the output of circuit 50 (i.e. during recovery of the diode) and supplies control terminal 13c with a given potential Vpol to set IGBT transistor 13 to an optimum linear operating region.

Claims

1. An electronic switching circuit (10) for reducing power-on switching transients, and comprising:

   - first electronic switching means (13) having first and second terminals (13a, 13b) communicating respectively with a supply voltage (Val) and a first terminal (15a) of a load (15), in particular a load comprising at least one inductive component (Lc);

   said first electronic switching means (13) having at least one control terminal (13c) controlled by a command signal (C) for alternately opening or closing said first switching means (13);

   - second electronic switching means (27) having first and second terminals (27a, 27b) communicating respectively with said first terminal (15a) of said load and with a second terminal (15b) of the load; and
   - recirculating diode means (30) located parallel with said second switching means (27);

   characterized by also comprising:

   - transducing means (33) cooperating with said recirculating diode means (30) and for generating a control signal (Vcnt) related to the rate of change of the current flowing in said recirculating diode means (30); and
   - active control means (17) interposed between a receiving input (17a) supplied with said command signal (C), and said control terminal (13c) of said first electronic switching means (13); said active control means (17) also receiving said control signal (Vcnt) to at least prevent said command signal (C) from being transferred to said control terminal (13c) of said first electronic switching means (13) to close the first switching means, when said control signal (Vcnt) assumes a predetermined relationship with respect to at least one threshold value (Vth).

2. A circuit as claimed in Claim 1, characterized in that said switching means comprise transistor means,

in particular IGBT transistors;

said active control means (17) comprising biasing means (70) which, upon said control signal (Vcnt) assuming said predetermined relationship, supply said control terminal (13c) of said first switching means (13) with a given potential (Vpol) for setting said transistor means (13) to a linear operating region.

3. A circuit as claimed in Claim 1 or 2, characterized in that said transducing means (33) are located in series with said first switching means (13).

4. A circuit as claimed in any one of the foregoing Claims, characterized in that said transducing means (33) comprise inductor means; said control signal (Vcnt) being defined by the voltage across said inductor means (33).

5. A circuit as claimed in any one of the foregoing Claims, characterized in that said active control means (17) comprise:

- comparing means (36) for comparing the control signal (Vcnt) with said threshold value, and generating a disabling signal (T2, V2) when said control signal (Vcnt) conforms with said predetermined relationship with respect to said threshold value (Vth); said comparing means (36) otherwise generating an enabling signal (T2, V2); and
- power-on control switching means (38) cooperating with said comparing means (36) and interposed between said control terminal and said receiving input; said power-on control switching means (38) being set, in the presence of said disabling signal (T2, V2), to an open state to prevent said command signal (C) from being transferred to said control terminal (13c) to close said first switching means (13);

said power-on control switching means (38) also being set, in the presence of said enabling signal (T2, V2), to a closed state to control said first switching means (13) by means of said command signal (C).

6. A circuit as claimed in Claim 5, characterized in that said power-on control switching means comprise:

- logic multiplying means (52) having a first input (52b) supplied with said command signal (C) varying between a first logic state (0) to open said first switching means (13), and a second logic state (1) to close said first switching means (13); said logic multiplying means (52) also having a second input (52a) communicating (50) with the output of said comparing means to alternately receive said disabling signal (V2) or said enabling signal (V2); said disabling signal representing a logic 0, in the presence of which said multiplying means generate a deenergizing signal for disabling closure of said first switching means (13).

7. A circuit as claimed in Claim 6, characterized by comprising level shifting means (54) interposed between said logic multiplying means (52) and said control terminal (13c), and for converting said deenergizing signal into a potential, in particular a floating potential, which is applied to said control terminal (13c) of said first electronic switching means to disable closure of said first switching means (13).

8. A circuit as claimed in Claim 6 or 7, characterized by comprising converting means (62) located parallel with said logic multiplying means (52), and which receive said control signal and convert said first logic state (0) of said command signal (C) into a command to open said first switching means (13).

9. A circuit as claimed in any one of the foregoing Claims, characterized in that said first electronic switching means comprise transistor means.

10. A circuit as claimed in any one of the foregoing Claims, characterized in that said first electronic switching means comprise an IGBT transistor.

11. A method of controlling an electronic switching circuit (10) comprising:

- first electronic switching means (13) having first and second terminals (13a, 13b) communicating respectively with a supply voltage (Val) and a first terminal (15a) of a load (15), in particular a load comprising at least one inductive component (Lc);

said first electronic switching means (13) having at least one control terminal (13c) controlled by a command signal (C) for alternately opening or closing said first switching means (13);

- second electronic switching means (27) having first and second terminals (27a, 27b) communicating respectively with said first terminal (15a) of said load and with a second terminal (15b) of the load; and
- recirculating diode means (30) located parallel with said second switching means (27);

characterized by comprising the steps of:

- generating a control signal (Vcnt) related to the rate of change of the current flowing in said re-

circulating diode means (30); and

- processing said control signal (Vcnt) to prevent said command signal (C) from being applied to said first electronic switching means (13) to close the first switching means, when said control signal (Vcnt) assumes a predetermined relationship with respect to at least one threshold value (Vth).

12. A method as claimed in Claim 11, characterized in that said processing step comprises the substeps of:

- comparing (36) the control signal (Vcnt) with said threshold value to generate a disabling signal (T2, V2) when said control signal (Vcnt) conforms with said predetermined relationship with respect to said threshold value (Vth), and to otherwise generate an enabling signal (V2);
- preventing said command signal (C) for closing said first electronic switching means (13) from being transferred, in the presence of said disabling signal (V2), to said control terminal (13c) of said first electronic switching means (13); and
- controlling said first switching means (13) by means of said command signal (C) in the presence of said enabling signal (V2).

13. A method as claimed in Claim 12, wherein said command signal (C) varies between a first logic state (0) to open said first switching means (13), and a second logic state (1) to close said first switching means (13);
characterized in that said processing step also comprises the step of:

- determining the logic product of said command signal (C) alternately multiplied by said disabling signal or said enabling signal; said disabling signal representing a logic 0 to generate, by means of said multiplication, a deenergizing signal for disabling closure of said first switching means (13).

Patentansprüche

1. Elektronischer Schaltkreis (10) zur Verringerung von Schaltstößen oder Einschwingvorgängen beim Einschalten, der folgendes aufweist:

- eine erste elektronische Schalteinrichtung (13), die einen ersten und einen zweiten Anschluß (13a, 13b) hat, die mit einer Versorgungsspannung (Val) bzw. einem ersten Anschluß (15a) einer Last (15) in Verbindung stehen, insbesondere einer Last, die wenigstens eine induktive Komponente (Lc) aufweist;

wobei die erste elektronische Schalteinrichtung (13) wenigstens einen Steueranschluß (13c) hat, der von einem Befehlssignal (C) so gesteuert wird, daß er die erste Schalteinrichtung (13) alternierend öffnet oder schließt;

- eine zweite elektronische Schalteinrichtung (27), die einen ersten und einen zweiten Anschluß (27a, 27b) hat, die mit dem ersten Anschluß (15a) der Last bzw. mit einem zweiten Anschluß (15b) der Last in Verbindung stehen; und
- eine Rückkopplungsdiodeneinrichtung (30), die zu der zweiten Schalteinrichtung (27) parallel angeordnet ist;

dadurch gekennzeichnet,
daß der Schaltkreis ferner folgendes aufweist:

- eine Wandlereinrichtung (33), die mit der Rückkopplungsdiodeneinrichtung (30) zusammenwirkt und ein Steuersignal (Vcnt) erzeugt, das von der Änderungsrate des in der Rückkopplungsdiodeneinrichtung (30) fließenden Stroms abhängt; und
- eine aktive Steuereinrichtung (17), die zwischen einem Empfangseingang (17a), dem das Befehlssignal (C) zugeführt wird, und dem Steueranschluß (13c) der ersten elektronischen Schalteinrichtung (13) angeordnet ist; wobei die aktive Steuereinrichtung (17) ebenfalls das Steuersignal (Vcnt) empfängt, um wenigstens zu verhindern, daß das Befehlssignal (C) zu dem Steueranschluß (13c) der ersten elektronischen Schalteinrichtung (13) übertragen wird, um die erste Schalteinrichtung zu schließen, wenn das Steuersignal (Vcnt) eine vorbestimmte Relation in bezug auf wenigstens einen Schwellenwert (Vth) annimmt.

2. Schaltkreis nach Anspruch 1,
dadurch gekennzeichnet,
daß die Schalteinrichtung eine Transistoreinrichtung, insbesondere IGBT-Transistoren, aufweist;
wobei die aktive Steuereinrichtung (17) eine Vorspannungseinrichtung (70) aufweist, die dann, wenn das Steuersignal (Vcnt) die vorbestimmte Relation annimmt, dem Steueranschluß (13c) der ersten Schalteinrichtung (13) ein gegebenes Potential (Vpol) zuführt, um die Transistoreinrichtung (13) auf einen linearen Betriebsbereich einzustellen.

3. Schaltkreis nach Anspruch 1 oder 2,
dadurch gekennzeichnet,
daß die Wandlereinrichtung (33) mit der ersten Schalteinrichtung (13) in Reihe angeordnet ist.

4. Schaltkreis nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet,
daß die Wandlereinrichtung (33) eine Induktionseinrichtung aufweist; wobei das Steuersignal (Vcnt) von der Spannung über der Induktionseinrichtung (33) gebildet wird.

5. Schaltkreis nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet,
daß die aktive Steuereinrichtung (17) folgendes aufweist:

- eine Vergleichseinrichtung (36) zum Vergleichen des Steuersignals (Vcnt) mit dem Schwellenwert und zum Erzeugen eines Sperrsignals (T2, V2), wenn das Steuersignal (Vcnt) mit der vorbestimmten Relation in bezug auf den Schwellenwert (Vth) übereinstimmt; wobei die Vergleichseinrichtung (36) anderenfalls ein Freigabesignal (T2, V2) erzeugt; und
- eine Einschaltsteuerungs-Schalteinrichtung (38), die mit der Vergleichseinrichtung (36) zusammenwirkt und zwischen dem Steueranschluß und dem Empfangseingang angeordnet ist; wobei die Einschaltsteuerungs-Schalteinrichtung (38) bei Anwesenheit des Sperrsignals (T2, V2) in einen offenen Zustand gesetzt wird, um zu verhindern, daß das Befehlssignal (C) zu dem Steueranschluß (13c) übertragen wird, um die erste Schalteinrichtung (13) zu schließen;

wobei die Einschaltsteuerungs-Schalteinrichtung (38) bei Anwesenheit des Freigabesignals (T2, V2) ferner in einen geschlossenen Zustand gesetzt wird, um die erste Schalteinrichtung (13) durch das Befehlssignal (C) zu steuern.

6. Schaltkreis nach Anspruch 5,
dadurch gekennzeichnet,
daß die Einschaltsteuerungs-Schalteinrichtung folgendes aufweist:

- eine logische Multiplikationseinrichtung (52), die einen ersten Eingang (52b) hat, dem das Befehlssignal (C) zugeführt wird, das zwischen einem ersten logischen Zustand (0) zum Öffnen der ersten Schalteinrichtung (13) und einem zweiten logischen Zustand (1) zum Schließen der ersten Schalteinrichtung (13) wechselt;

wobei die logische Multiplikationseinrichtung (52) ferner einen zweiten Eingang (52a) hat, der mit dem Ausgang der Vergleichseinrichtung in Verbindung steht (50), um alternierend das Sperrsignal (V2) oder das Freigabesignal (V2) zu empfangen; wobei das Sperrsignal eine logische 0 repräsentiert, bei deren Anwesenheit die Multiplikationseinrichtung ein Desaktivierungssignal zum Sperren des Schließens der ersten Schalteinrichtung (13) erzeugt.

7. Schaltkreis nach Anspruch 6,
dadurch gekennzeichnet,
daß er eine Pegelverschiebungseinrichtung (54) aufweist, die zwischen der logischen Multiplikationseinrichtung (52) und dem Steueranschluß (13c) angeordnet ist und das Desaktivierungssignal in ein Potential, insbesondere ein Floating-Potential, umwandelt, das an den Steueranschluß (13c) der ersten elektronischen Schalteinrichtung angelegt wird, um das Schließen der ersten Schalteinrichtung (13) zu sperren.

8. Schaltkreis nach Anspruch 6 oder 7,
dadurch gekennzeichnet,
daß er eine Umwandlungseinrichtung (62) aufweist, die zu der logischen Multiplikationseinrichtung (52) parallel angeordnet ist und die das Steuersignal empfängt und den ersten logischen Zustand (0) des Befehlssignals (C) in einen Befehl zum Öffnen der ersten Schalteinrichtung (13) umwandelt.

9. Schaltkreis nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet,
daß die erste elektronische Schalteinrichtung eine Transistoreinrichtung aufweist.

10. Schaltkreis nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet,
daß die erste elektronische Schalteinrichtung einen IGBT-Transistor aufweist.

11. Verfahren zum Steuern einer elektronischen Schalteinrichtung (10), die folgendes aufweist:

- eine erste elektronische Schalteinrichtung (13), die einen ersten und einen zweiten Anschluß (13a, 13b) hat, die mit einer Versorgungsspannung (Val) bzw. einem ersten Anschluß (15a) einer Last (15) in Verbindung stehen, insbesondere einer Last, die wenigstens eine induktive Komponente (Lc) aufweist;
- wobei die erste elektronische Schalteinrichtung (13) wenigstens einen Steueranschluß (13c) hat, der von einem Befehlssignal (C) so gesteuert wird, daß er die erste Schalteinrichtung (13) alternierend öffnet oder schließt;
- eine zweite elektronische Schalteinrichtung (27), die einen ersten und einen zweiten Anschluß (27a, 27b) hat, die mit dem ersten Anschluß (15a) der Last bzw. mit einem zweiten

Anschluß (15b) der Last in Verbindung stehen; und

- eine Rückkopplungsdiodeneinrichtung (30), die zu der zweiten Schalteinrichtung (27) parallel angeordnet ist;

dadurch gekennzeichnet,
daß das Verfahren die folgenden Schritte aufweist:

- Erzeugen eines Steuersignals (Vcnt), das von der Änderungsrate des in der Rückkopplungsdiodeneinrichtung (30) fließenden Stroms abhängt; und
- Verarbeiten des Steuersignals (Vcnt), um zu verhindern, daß das Befehlssignal (C) an die erste elektronische Schalteinrichtung (13) angelegt wird, um die erste Schalteinrichtung zu schließen, wenn das Steuersignal (Vcnt) eine vorbestimmte Relation in bezug auf wenigstens einen Schwellenwert (Vth) annimmt.

12. Verfahren nach Anspruch 11,
dadurch gekennzeichnet,
daß der Verarbeitungsschritt die folgenden Teilschritte aufweist:

- Vergleichen (36) des Steuersignals (Vcnt) mit dem Schwellenwert, um ein Sperrsignal (T2, V2) zu erzeugen, wenn das Steuersignal (Vcnt) mit der vorbestimmten Relation in bezug auf den Schwellenwert (Vth) übereinstimmt, und um anderenfalls ein Freigabesignal (V2) zu erzeugen;
- Verhindern, daß das Befehlssignal (C) zum Schließen der ersten elektronischen Schalteinrichtung (13) bei Anwesenheit des Sperrsignals (V2) zu dem Steueranschluß (13c) der ersten elektronischen Schalteinrichtung (13) übertragen wird; und
- Steuern der ersten Schalteinrichtung (13) durch das Befehlssignal (C) bei Anwesenheit des Freigabesignals (V2).

13. Verfahren nach Anspruch 12,
wobei das Befehlssignal (C) zwischen einem ersten logischen Zustand (0) zum Öffnen der ersten Schalteinrichtung (13) und einem zweiten logischen Zustand (1) zum Schließen der ersten Schalteinrichtung (13) wechselt; dadurch gekennzeichnet,
daß der Verarbeitungsschritt ferner die folgenden Schritte aufweist:

- Bestimmen des logischen Produkts des Befehlssignals (C), das alternierend mit dem Sperrsignal oder dem Freigabesignal multipliziert wird; wobei das Sperrsignal eine logische 0 repräsentiert, um durch die Multiplikation ein Desaktivierungssignal zum Sperren des Schließens der ersten Schalteinrichtung (13) zu erzeugen.

Revendications

1. Circuit de commutation électronique (10) pour réduire les transitoires de commutation à la mise sous tension, et comprenant :

- des premiers moyens de commutation électronique (13) ayant des première et deuxième bornes (13a, 13b) communiquant respectivement avec une tension d'alimentation (Va1) et une première borne (15a) d'une charge (15), en particulier une charge comprenant au moins un composant inductif (Lc) ;

lesdits moyens de commutation électronique (13) ayant au moins une borne de commande (13c) commandée par un signal de commande (C) pour ouvrir ou fermer en alternance lesdits premiers moyens de commutation (13) ;

- des seconds moyens de commutation électronique (27) ayant des première et deuxième bornes (27a, 27b) communiquant respectivement avec ladite première borne (15a) de ladite charge et avec une seconde borne (15b) de la charge ; et
- des moyens formant diode à circulation (30) situés en parallèle auxdits seconds moyens de commutation (27) ;

caractérisé par le fait qu'il comprend également :

- des moyens formant transducteur (33) coopérant avec lesdits moyens formant diode à circulation (30) et pour produire un signal de commande (Vcnt) se rapportant à la vitesse de modification du courant s'écoulant dans lesdits moyens formant diode à circulation (30) ; et
- des moyens de commande active (17) interposés entre une entrée de réception (17a) alimentée par ledit signal de commande (C), et ladite borne de commande (13c) desdits premiers moyens de commutation électronique (13) ; lesdits moyens de commande active (17) recevant également ledit signal de commande (Vcnt) pour au moins empêcher ledit signal de commande (C) d'être transféré vers ladite borne de commande (13c) desdits premiers moyens de commutation électronique (13) pour fermer les premiers moyens de commutation, quand ledit signal de commande (Vcnt) prend une relation prédéterminée par rapport à au

moins une valeur de seuil (Vth).

2. Circuit selon la revendication 1, caractérisé en ce que lesdits moyens de commutation comprennent des moyens formant transistor, en particulier des transistors IGBT ;

lesdits moyens de commande active (17) comprenant des moyens de polarisation (70) qui, lorsque ledit signal de commande (Vcnt) prend ladite relation prédéterminée, alimentent ladite borne de commande (13c) desdits premiers moyens de commutation (13) par un potentiel donné (Vpo1) pour mettre lesdits moyens formant transistor (13) dans une zone de fonctionnement linéaire.

3. Circuit selon la revendication 1 ou 2, caractérisé en ce que lesdits moyens formant transducteur (33) sont situés en série avec lesdits premiers moyens de commutation (13).

4. Circuit selon l'une quelconque des revendications précédentes, caractérisé en ce que lesdits moyens formant transducteur (33) comprennent des moyens formant bobine d'inductance ; ledit signal de commande (Vcnt) étant défini par la tension aux bornes desdits moyens formant bobine d'inductance (33).

5. Circuit selon l'une quelconque des revendications précédentes, caractérisé en ce que lesdits moyens de commande active (17) comprennent :

- des moyens de comparaison (36) pour comparer le signal de commande (Vcnt) à ladite valeur de seuil, et pour produire un signal d'invalidation (T2, V2) lorsque ledit signal de commande (Vcnt) est conforme à ladite relation prédéterminée par rapport à ladite valeur de seuil (Vth) ; lesdits moyens de comparaison (36) produisant autrement un signal de validation (T2, V2) ; et
- des moyens de commutation de commande de mise sous tension (38) coopérant avec lesdits moyens de comparaison (36) et interposés entre ladite borne de commande et ladite entrée de réception ; lesdits moyens de commutation de commande de mise sous tension (38) étant mis, en présence dudit signal d'invalidation (T2, V2), dans un état ouvert pour empêcher ledit signal de commande (C) d'être transféré vers ladite borne de commande (13c) pour fermer lesdits premiers moyens de commutation (13) ;

lesdits moyens de commutation de commande de mise sous tension (38) étant également mis, en présence dudit signal de validation (T2, V2), dans un état fermé pour commander lesdits premiers moyens de commutation (13) au moyen dudit signal de commande (C).

6. Circuit selon la revendication 5, caractérisé en ce que lesdits moyens de commutation de commande de mise sous tension comprennent :

- des moyens de multiplication logique (52) ayant une première entrée (52b) alimentée par ledit signal de commande (C) variant entre un premier état logique (0) pour ouvrir lesdits premiers moyens de commutation (13), et un second état logique (1) pour fermer lesdits premiers moyens de commutation (13) ; lesdits moyens de multiplication logique (52) ayant également une seconde entrée (52a) communiquant (50) avec la sortie desdits moyens de comparaison pour recevoir en alternance ledit signal d'invalidation (V2) ou ledit signal de validation (V2) ; ledit signal d'invalidation représentant un niveau logique 0, en présence duquel lesdits moyens de multiplication produisent un signal de désexcitation pour invalider la fermeture desdits premiers moyens de commutation (13).

7. Circuit selon la revendication 6, caractérisé en ce qu'il comprend des moyens de décalage de niveau (54) interposés entre lesdits moyens de multiplication logique (52) et ladite borne de commande (13c), et pour transformer ledit signal de désexcitation en un potentiel, en particulier un potentiel flottant, qui est appliqué à ladite borne de commande (13c) desdits premiers moyens de commutation électronique pour invalider la fermeture desdits premiers moyens de commutation (13).

8. Circuit selon la revendication 6 ou 7, caractérisé en ce qu'il comprend des moyens de transformation (62) situés en parallèle auxdits moyens de multiplication logique (52), et qui reçoivent ledit signal de commande et qui transforment ledit premier état logique (0) dudit signal de commande (C) en une commande pour ouvrir lesdits premiers moyens de commutation (13).

9. Circuit selon l'une quelconque des revendications précédentes, caractérisé en ce que lesdits premiers moyens de commutation électronique comprennent des moyens formant transistor.

10. Circuit selon l'une quelconque des revendications précédentes, caractérisé en ce que lesdits premiers moyens de commutation électronique comprennent un transistor IGBT.

11. Procédé de commande d'un circuit de commutation électronique (10) comprenant :

- des premiers moyens de commutation électronique (13) ayant des première et deuxième bornes (13a, 13b) communiquant respectivement avec une tension d'alimentation (Va1) et une première borne (15a) d'une charge (15), en particulier une charge comprenant au moins un composant inductif (Lc) ;

lesdits moyens de commutation électronique (13) ayant au moins une borne de commande (13c) commandée par un signal de commande (C) pour ouvrir ou fermer en alternance lesdits premiers moyens de commutation (13) ;

- des seconds moyens de commutation électronique (27) ayant des première et deuxième bornes (27a, 27b) communiquant respectivement avec ladite première borne (15a) de ladite charge et avec une seconde borne (15b) de la charge ; et
- des moyens formant diode à circulation (30) situés en parallèle auxdits seconds moyens de commutation (27) ;

caractérisé par le fait qu'il comprend les étapes suivantes :

- la production d'un signal de commande (Vcnt) se rapportant à la vitesse de modification du courant s'écoulant dans lesdits moyens formant diode à circulation (30) ; et
- le traitement dudit signal de commande (Vcnt) pour empêcher ledit signal de commande (C) d'être appliqué auxdits premiers moyens de commutation électronique (13) pour fermer les premiers moyens de commutation, quand ledit signal de commande (Vcnt) prend une relation prédéterminée par rapport à au moins une valeur de seuil (Vth).

12. Procédé selon la revendication 11, caractérisé en ce que ladite étape de traitement comprend les étapes secondaires suivantes :

- la comparaison (36) du signal de commande (Vcnt) à ladite valeur de seuil pour produire un signal d'invalidation (T2, V2) lorsque ledit signal de commande (Vcnt) est conforme à ladite relation prédéterminée par rapport à ladite valeur de seuil (Vth), et pour produire autrement un signal de validation (V2) ;
- empêcher ledit signal de commande (C) de fermeture desdits premiers moyens de commutation électronique (13) d'être transféré, en présence dudit signal d'invalidation (V2), vers ladite borne de commande (13c) desdits premiers moyens de commutation électronique (13) ; et
- la commande desdits premiers moyens de commutation (13) au moyen dudit signal de commande (C), en présence dudit signal de validation (V2).

13. Procédé selon la revendication 12, dans lequel ledit signal de commande (C) varie entre un premier état logique (0) pour ouvrir lesdits premiers moyens de commutation (13), et un second état logique (1) pour fermer lesdits premiers moyens de commutation (13) ;

caractérisé en ce que ladite étape de traitement comprend également l'étape suivante :

- la détermination du produit logique dudit signal de commande (C) multiplié en alternance par ledit signal d'invalidation ou ledit signal de validation ; ledit signal d'invalidation représentant un niveau logique 0 pour produire, au moyen de ladite multiplication, un signal de désexcitation pour invalider la fermeture desdits premiers moyens de commutation (13).

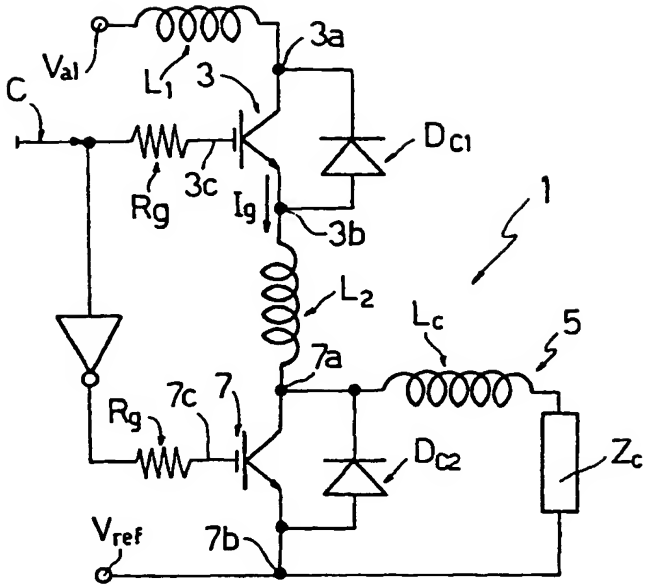

Fig.1

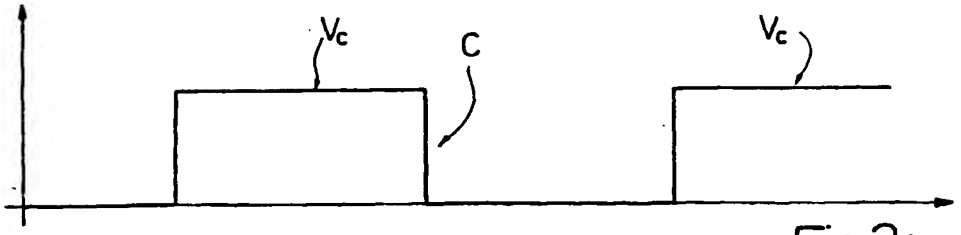

Fig.2a

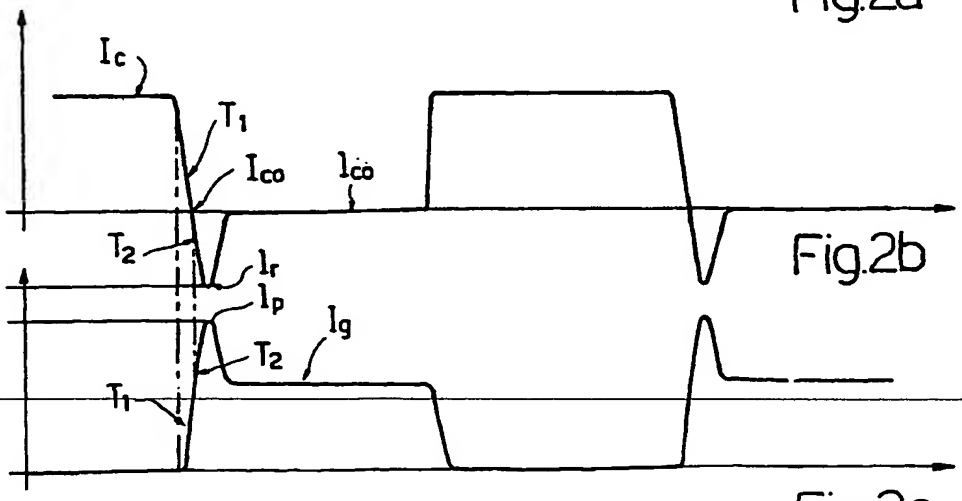

Fig.2b

Fig.2c

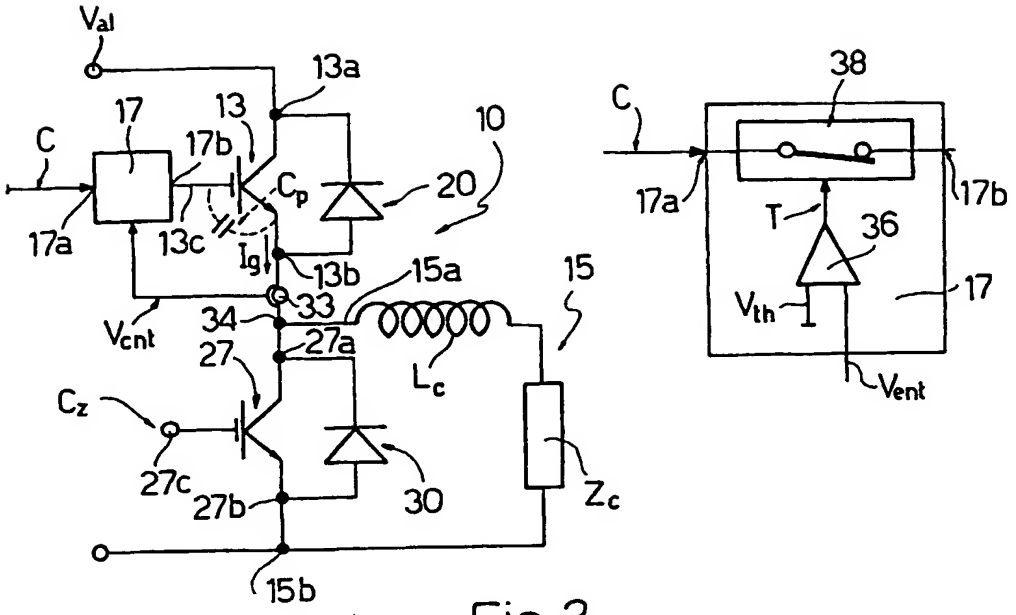

Fig.3

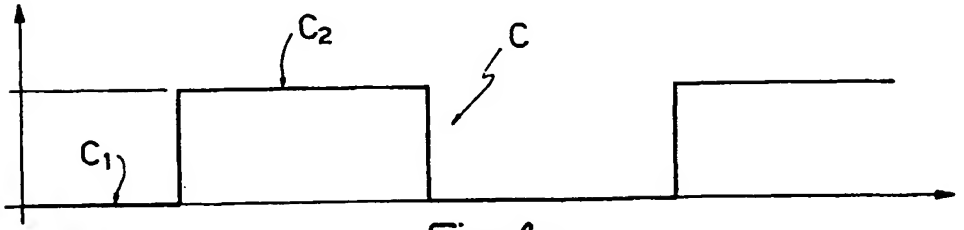

Fig.4a

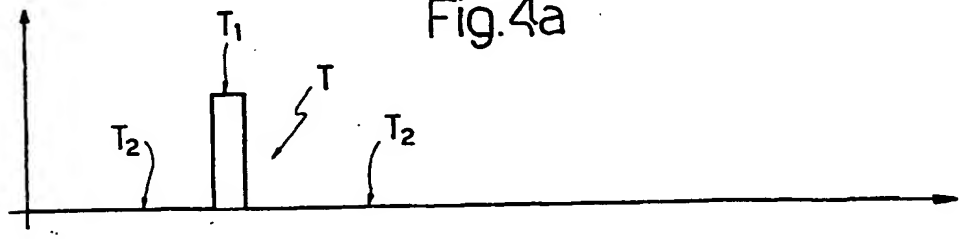

Fig.4b

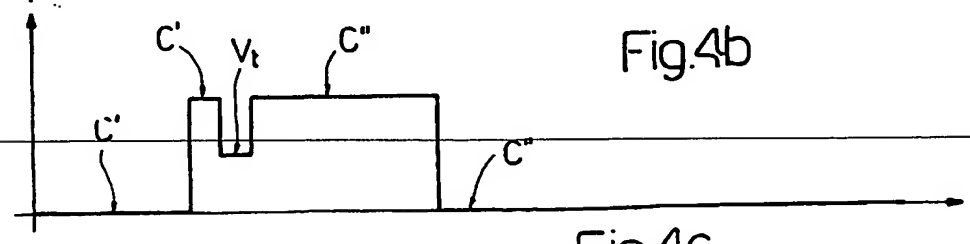

Fig.4c

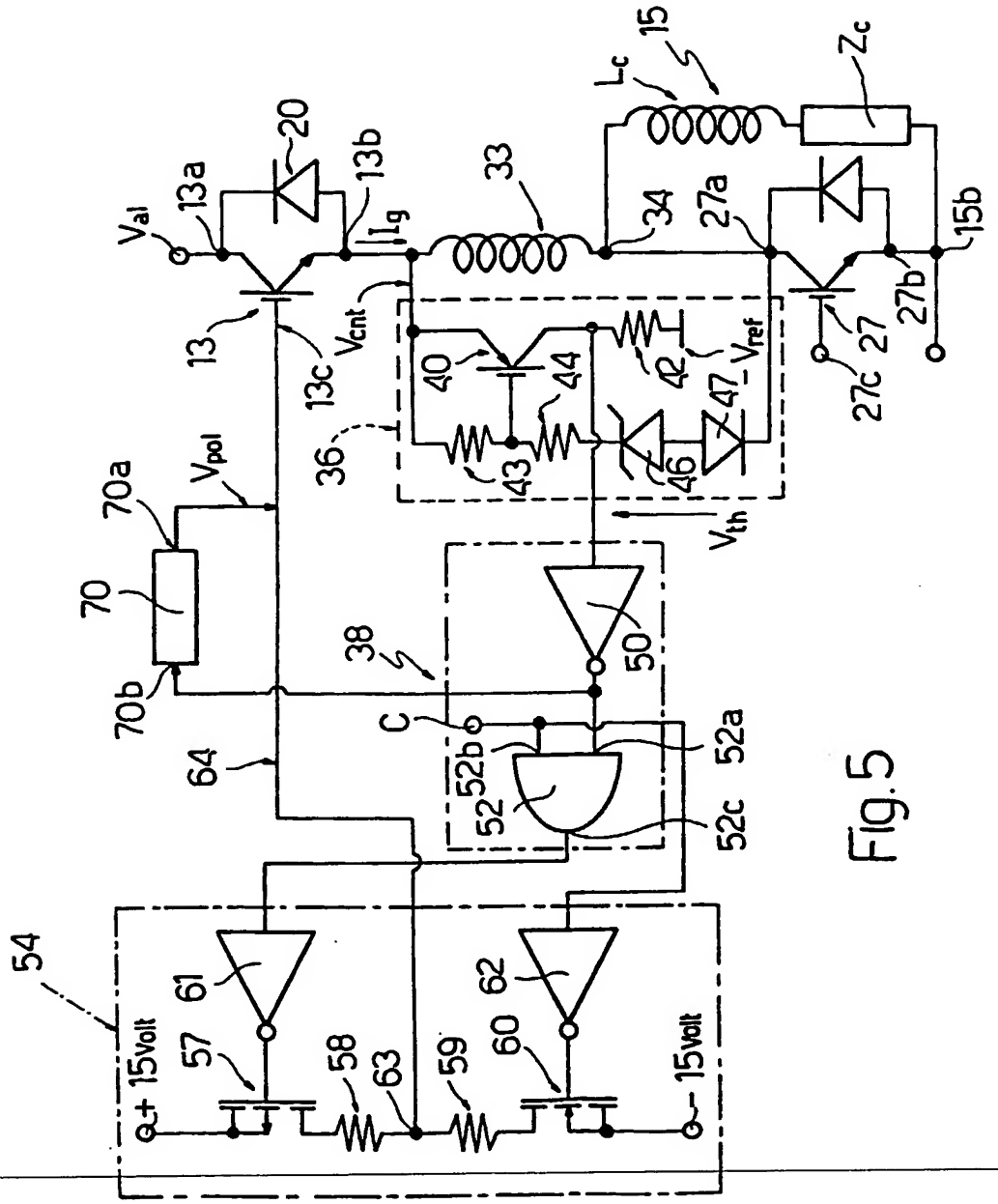
Lc
15
Zc
20
13a
13b
33
Val
Ig
34
27a
15b
13
Vcnt
13c
40
44
42
Vref
47
27c
27
27b
36
43
46
Vpol
70a
70
Vth
38
50
70b
C
64
52b
52a
52
52c
54
61
62
57
58
63
59
60
+15volt
-15volt

Fig.5

Fig.6a

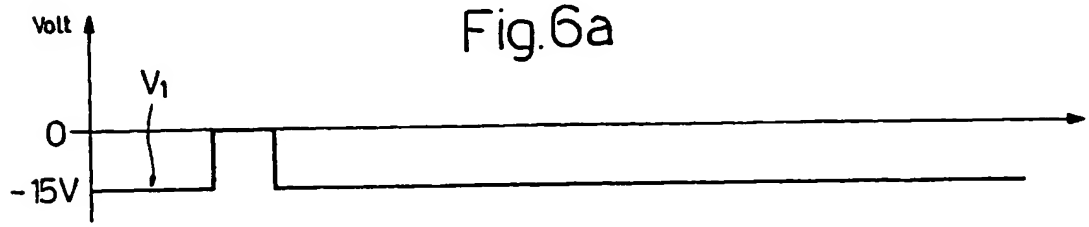

Fig.6b

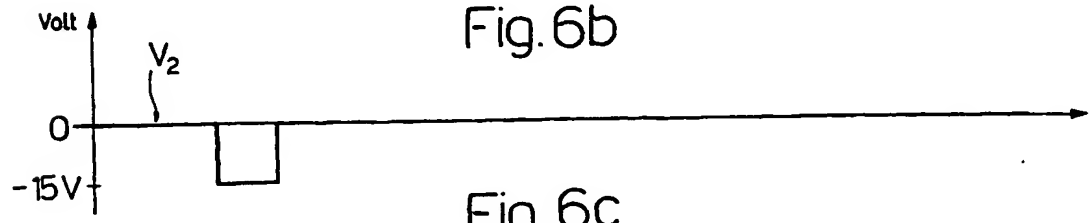

Fig. 6c

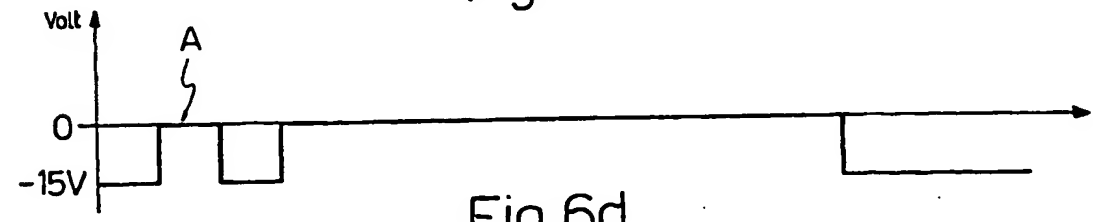

Fig. 6d

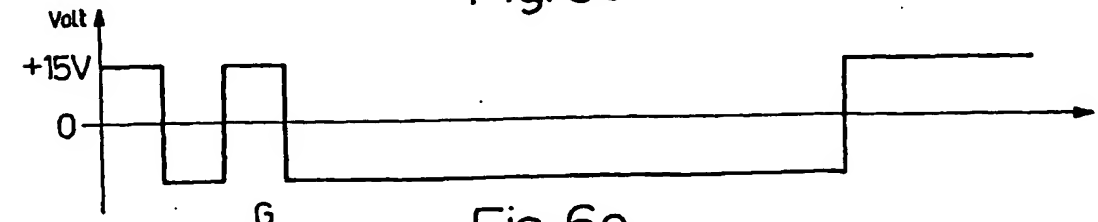

Fig. 6e

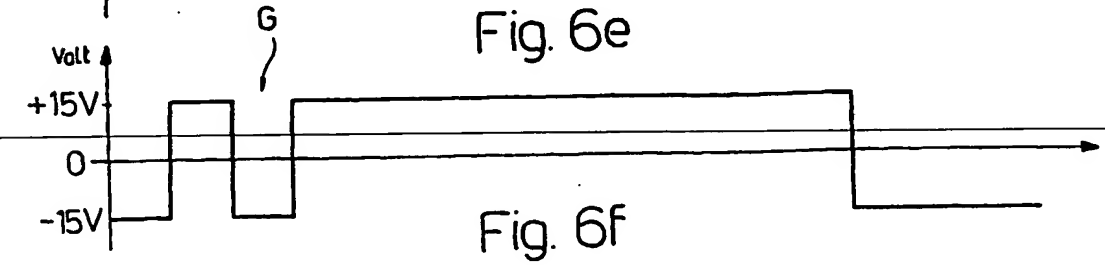

Fig. 6f